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Analysis of Physical Characteristics of Hybrid Materials-based MOSFETs Design

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Abstract:

The paper presents the research on physical characteristics of hybrid materials-based MOSFETs design. The research problem in this study is to understand the theoretical approach-based real device fabrication. The objective of this study is to investigate the physical characteristics of the hybrid material-based MOSFET structure. An analytical physics-based compact model of hybrid materials-based MOSFET, which can accurately describe the I-V characteristics in all operation modes have been presented in this paper. The model considers the source-drain resistance, different interface trap densities and self-heating effects. The analyses are conducted by using MATLAB language.

Keywords:

Physical Characteristics, Hybrid Material, MOSFET, Semiconductor Electronics, Numerical Analysis

1. Introduction

Hybrid Materials-based transistor technology has many advantages that make it a promising candidate for high-speed power electronics. It allows high-power operation at much higher frequencies than silicon laterally diffused metal-oxide-semiconductor field-effect transistors (LDMOSFETs), currently a staple for the cellular base station industry [1]. The high breakdown voltage capability (over 100 V), high electron mobility, and high-temperature performance of Hybrid Materials-based MOSFET are the main factors for its use in power electronics applications. Circuits design in both application regimes requires the accurate compact device models that can describe the non-linear I-V characteristics. The current state-of-the-art Hybrid Materials-based power transistor circuit models are mostly empirical in nature and contain a large number of fitting parameters. The source-drain series resistance and self-heating make the compact modelling difficult [2]. Currently available models are not enough accurate to describe the I-V characteristics of power Hybrid Materials-based MOSFET in all operation modes. This means, that we need a compact physics-based analytical model based on the physical description of the device. In this paper, we present a physics-based Hybrid Materials-based power transistor model based on generic approach. The paper contains 3 parts. In the first part, we will give a concise

description of the model. The effects of specific power Hybrid Materials-based MOSFET, such as series resistance and self-heating will be discussed in the second and third parts.

2. Background Description of the MOSFET Model

Presented in this paper model relies on the diffusion-drift transistor model, originally proposed in [3,4]. This model is based on an explicit solution of the channel current continuity equation, and it has been consistently realized for different type's field-effect devices including SOI and double-gate transistors [5], graphene FETs [6], and molybdenite MoS2 monolayer transistor [7]. This model is able to describe via a single analytic expression the whole I-V characteristics both in subthreshold and above threshold regions and in linear and saturation modes. Generic form I-V characteristics of an ideal (i.e., without any geometrical short-channel effects) FET in a concise form:

$$I_D = I_{DSAT}\left(1-\exp\left(-2\frac{V_{DS}}{V_{DSAT}}\right)\right) \tag{1}$$

where I_{DSAT} is the saturation current, V_{DS} is the drain-source bias. The drain saturation voltage V_{DSAT} is an explicit function of the mobile charge density:

$$V_{DSAT} \cong \varphi_T\left(1+\frac{C_{it}}{C_{ox}+C_D}\right)+\frac{qn_{s0}}{C_{ox}+C_D} \tag{2}$$

where q is the electron charge, n_{S0} is the channel carrier density near the source, $\varphi_T = \frac{k_B T}{q}$ is the thermal potential, C_{ox}, C_D are the oxide and the depletion layer capacitance per unit area, correspondingly. The MOSFET electrostatic saturation current I_{DSAT} is represented as a sum of the diffusion and the drift components [8]:

$$I_{DSAT} = \frac{W}{L} qD_0 n_{s0} + \frac{W}{L}\frac{\mu_0 q^2 n_{s0}^2}{2(C_{ox}+C_D)} \tag{3}$$

where W and L are the channel's width and length, q is the electron charge, μ_0 and D_0 are the channel carrier mobility and diffusivity, coupled by the Einstein relation $D_0 = \mu_0 \varphi_T$ .The first term in (3), corresponding to a linear dependence of the drain current on n_{S0}, is a diffusion current, dominating in the subthreshold region at low n_{S0}. The second term in (3) corresponds to the saturated drift current in the above-threshold mode in a well-known square-law approximation [9]. The dependence on the gate voltage V_G has in (1) an implicit form via the dependence n_{S0} (V_G). A concrete form of n_{S0} (V_G) should be determined by electrostatic consideration, which is different for different device configurations (bulk or SOI FETs, double gate FETs, FinFETs etc.):

$$I_D = \frac{W}{L} e\mu_0 n_{s0} V_{DS} \equiv G_D V_{DS} \tag{4}$$

where G_D is the channel conductance (i.e. total inverse channel resistance at low drain bias) in a low drain bias regime:

$$G_D = \frac{W}{L} e\mu_0 n_{s0} \tag{5}$$

3. Analysis and Discussions

The numerical analysis on proposed system and discussions on the simulation results have been completed in this section.

Channel Carrier Density as Function of Gate Voltage

We will use a phenomenological interpolation for $n_{S0}(V_G)$ which is similar to that used in CMOS design compact model BSIM [10]:

$$en_{s0}=\frac{2C_1S\ln\left[1+\exp\left(\frac{V_G-V_T}{2S}\right)\right]}{1+2\frac{C_1S}{C_1\varphi_T}\exp\left(\frac{V_G-V_T}{2S}\right)} \tag{6}$$

where V_T is the threshold voltage, C_1 (C_2) is the effective gate-to-channel capacitance per unit area in the above threshold (subthreshold) operation modes, $S=dV_G/d(\ln I_D)$ is the logarithmic subthreshold slope [9] which to be fitted from the sub-threshold part of the I-V curve. The interpolation (6) is validated by its asymptotic in the subthreshold and above-threshold regions (note $SS\equiv \ln 10S$):

$$en_{s0}\cong\begin{cases}C_1(V_G-V_T), & V_G>V_T\\ C_2\varphi_T\left(\frac{V_G-V_T}{S}\right)=C_2\varphi_T 10^{\frac{V_G-V_T}{S}}, & V_G<V_T\end{cases} \tag{7}$$

In GaAs FET the subthreshold slope is strongly dependent on the drain voltage:

$$S=S_0+m_dV_{DS} \tag{8}$$

where S_0 (~ 90-120 mV/decade) is the constant subthreshold slope extracted at small V_{DS}, m_d (~0.01-0.2) is a fitting constant. The threshold voltage is dependent on V_{DS} via the so-called DIBL (Drain- Induced Barrier Lowering) effect:

$$V_T=V_{T0}-\alpha_{DIBL}V_{DS} \tag{9}$$

where V_{T0} is a constant threshold voltage, α_{DIBL} is a DIBL sensitivity parameter.

3.1. Accounting for Series Resistance

Most of the state-of-the-art powers FETs are not self-aligned and their access regions affect device performance. The external drain voltage V_D can be written as a sum of internal channel voltage V_D^{int} and the voltage on R_D:

$$V_D^{int}=V_D-I_DR_D \tag{10}$$

where R+ is the drain resistance. Taking into account the equation (1), one can rewrite (10) as follows:

$$\frac{V_D-V_D^{int}}{R_D}=I_{DSAT}(V_G)\left[1-\exp\left(-2\frac{V_{DS}^{int}}{V_{DSAT}(V_G)}\right)\right] \tag{11}$$

Where:

$$I_{DSAT}=\frac{1}{2}G_DV_{DSAT} \tag{12}$$

From the equation (11) we have the exact solution for the drain current:

$$I_D\cong I_{DSAT}\left[1-\frac{1}{s}W\left(s\exp\left[s-\frac{2V_{DS}}{V_{DSAT}}\right]\right)\right] \tag{13}$$

where $s=G_DR_D$, W(s) is the Lambert function, defined as a solution of the equation:

$$W(se^s)=s \tag{14}$$

3.2. Analysis on Self-heating Effects

The problem of self-heating in power Hybrid Materials-based MOSFET is a severe issue that that affects the device reliability and degrades the I-V characteristics [9]. The carrier mobility at room and elevated temperatures T is mainly determined by phonons, and it can be simulated as to be proportional to T^{-n} where n is a parameter (~1.0-1.5). Mobility is generally reducing the temperature due to phonon scattering:

$$\mu_0(T) \propto \left(\frac{T_0}{T_0+\Delta T}\right)^n \propto 1-n\frac{\Delta T}{T_0} \tag{15}$$

where T_0 is a nominal operating temperature. We will model the self-heating effects through the following self-consistent equation:

$$I_D(T_0+\Delta T)V_{DS}R_{th}=\Delta T \tag{16}$$

where R_{th} is the thermal resistance (~ 30 K/W). From the equation (16) one gets:

$$I_D(T_0)\left[1-n\frac{\Delta T}{T_0}\right] \cong \frac{\Delta T}{V_{DS}R_{th}} \tag{17}$$

$$\Delta T \cong I_D(T_0)\frac{V_{DS}R_{th}}{nI_D(T_0)V_{DS}R_{th}+1} \tag{18}$$

Here, n can be considered as a fitting dimensionless parameter of order unity. Substituting (19) to the equation (17), the drain current with self-heating effects $\bar{I}_D$ can be approximated by the following relationship:

$$\bar{I}_D=I_D(T_0+\Delta T)\cong I_D(T_0)-n\frac{I_D(T_0)}{T_0}\Delta T=\frac{I_D(T_0)}{1+\frac{nI_D(T_0)V_{DS}R_{th}}{T_0}} \tag{19}$$

3.3. Results

There are three all-purpose characteristics of hybrid materials-based MSFET devices. Figure 1 demonstrates the I-V Characteristics of MOSFET. When the channel of MOSFET is turned off, no current could surge between the source and drain, consequently the current is zero. The entire gate voltages that are such that they do not turn the channel on result in fundamentally zero drain current. There is a linear area at low drain-source voltages. The drain current is comparative to the drain-source voltage. The slope depends on the functional gate voltage.

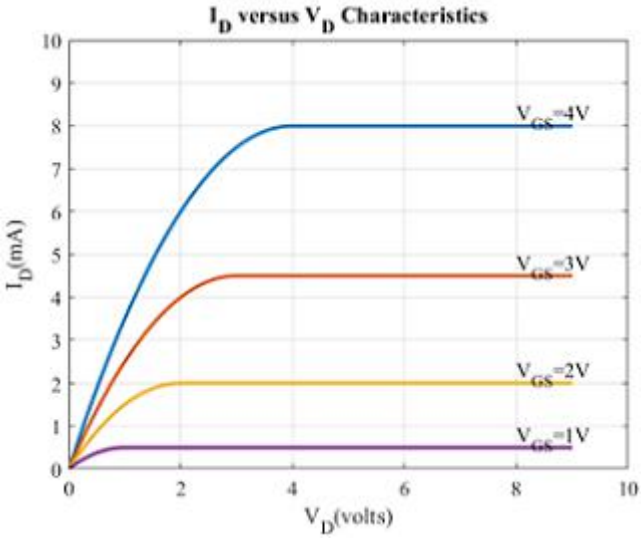

Figure 1. *Voltage-Current Characteristics of Hybrid Materials-based MOSFET.*

At higher drain-source voltages, the drain current turns into “saturated”. The current is no longer relative to the drain-source voltage, and as an alternative happen to approximately constant. This current is on the other hand strappingly reliant on the gate voltage.

4. Conclusion

The goal has been to provide a description of the power Hybrid Materials-based MOSFET compact analytical model, which is capable of simulating in a unified manner all the MOSFET’s operation modes using a compact and transparent analytical relationship. It has been shown that the model is suitable for accurate simulation of the Hybrid Materials-based I-V characteristics in modern power MOSFET circuits. The simulation results show that the analytical model is useful for describing the I-V characteristics, taking into account the drain resistance and self-heating effects.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this article.

Author Contributions

This study mainly focuses on the physical characteristics of hybrid materials-based MOSFETs design. The theoretical analyses on mathematical modelling for MOSFET Structure are vital role to enhance the high performance device fabrication for future semiconductor technology. This work could be provided to find the solution for research problems in advanced modelling techniques for power devices in reality.

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